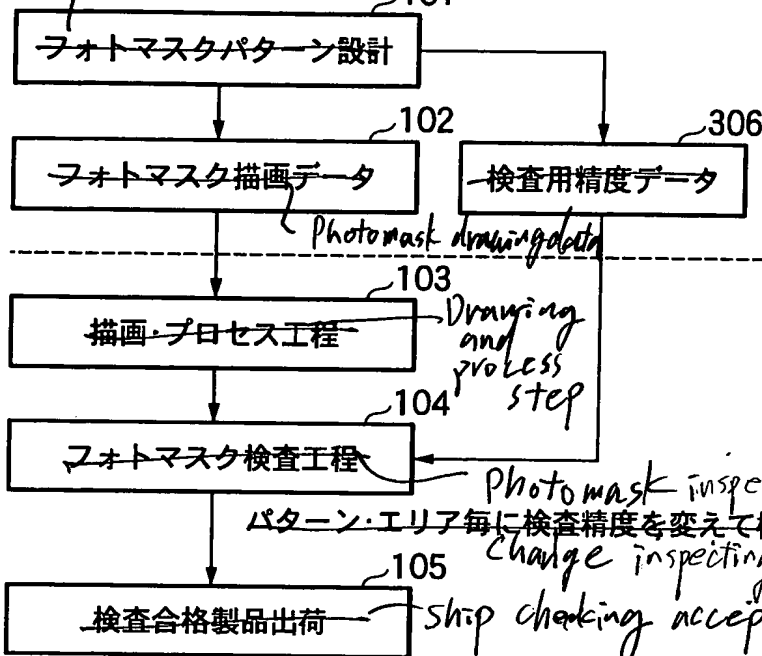


【書類名】 図面

【図1】 Design photomask pattern

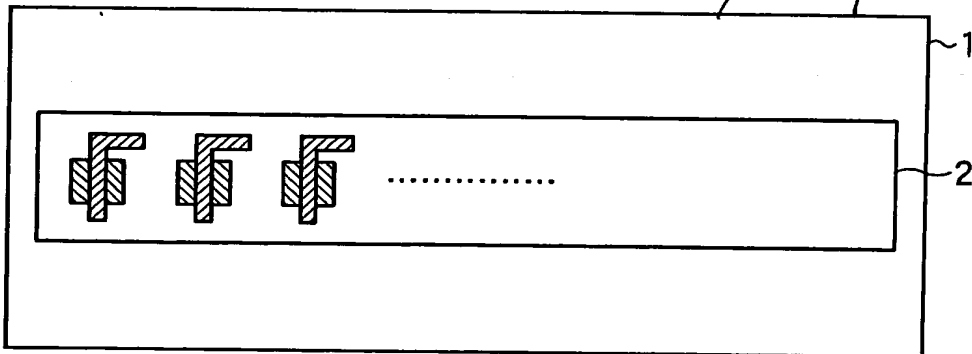
Fig. 1



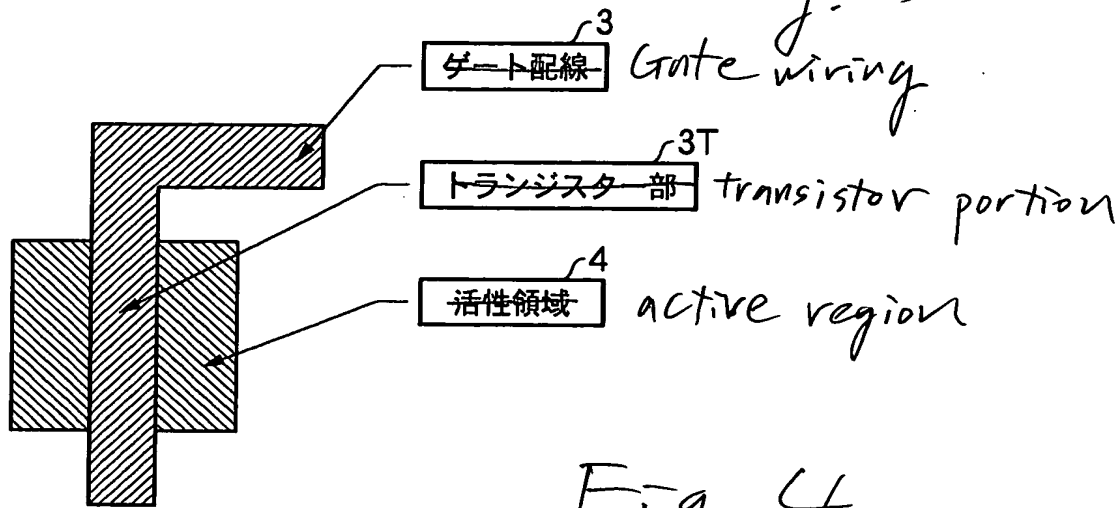
【図2】

Fig. 2

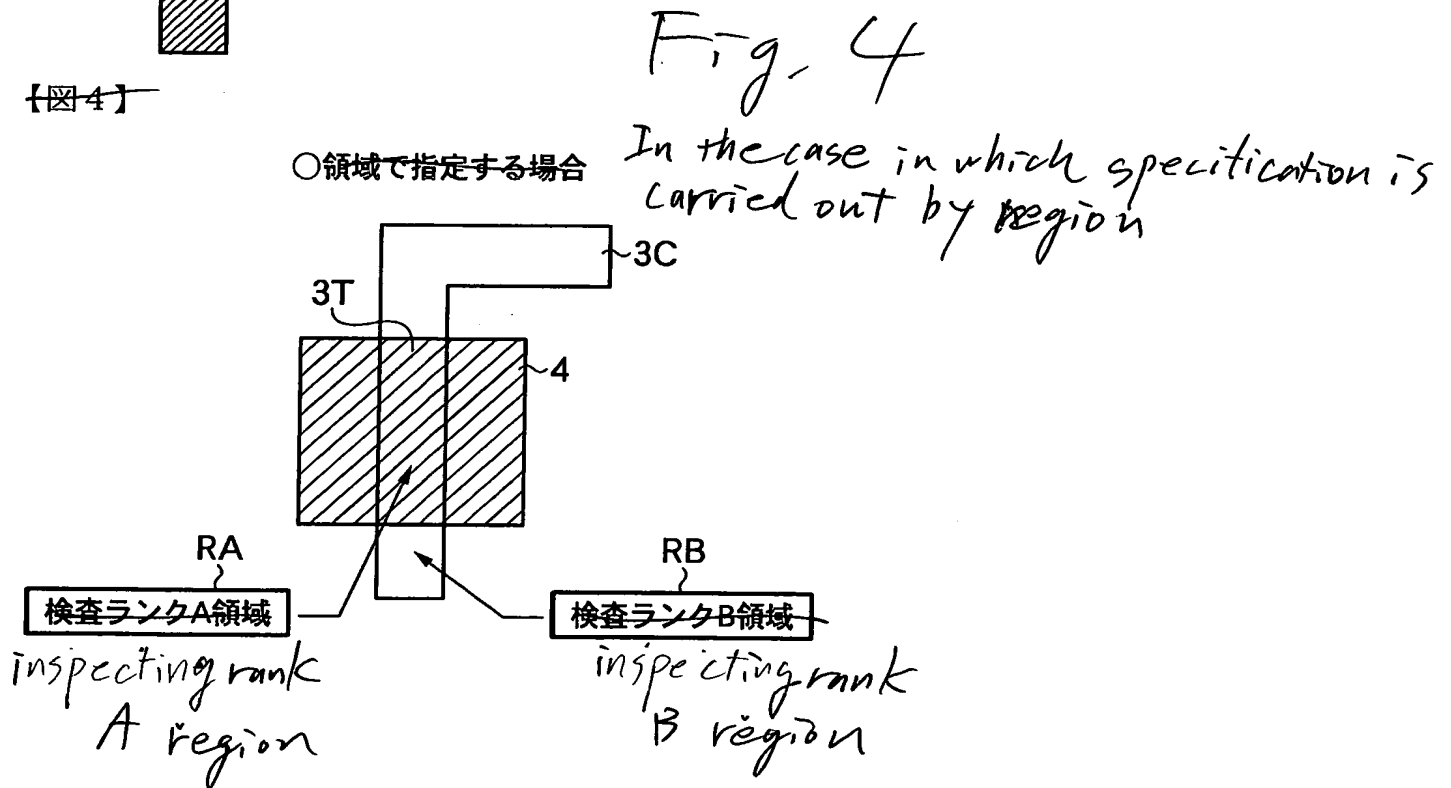
トランジスタアレイチップ Transistor array chip



【図3】

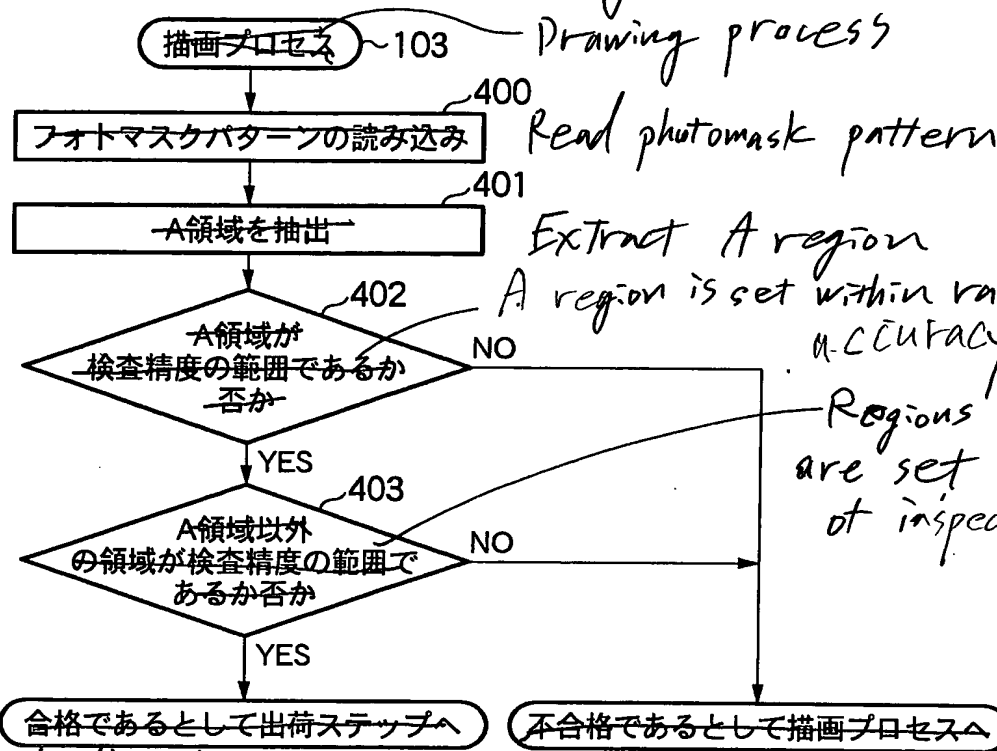


【図4】



【図5】

Fig. 5

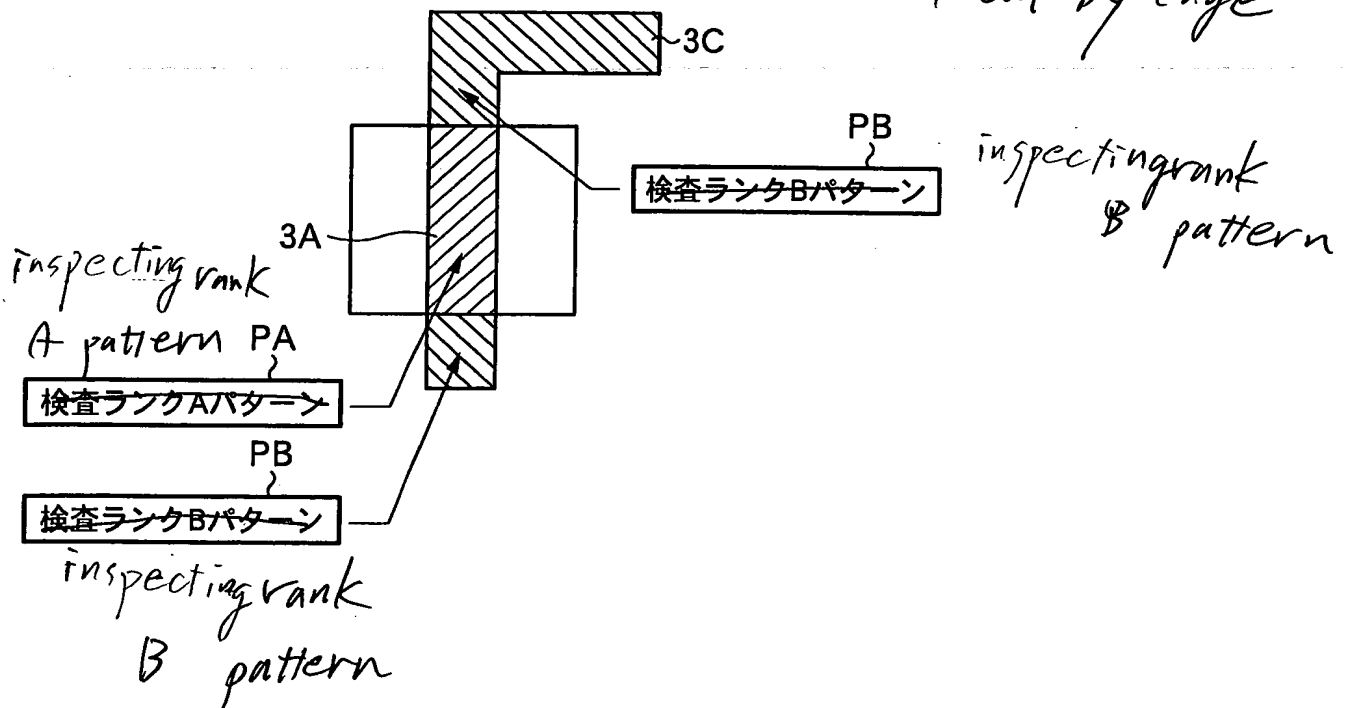


To shipping step for "accepted"

To drawing process for "rejected"

○パターンで指定する場合

In the case in which specification is carried out by edge

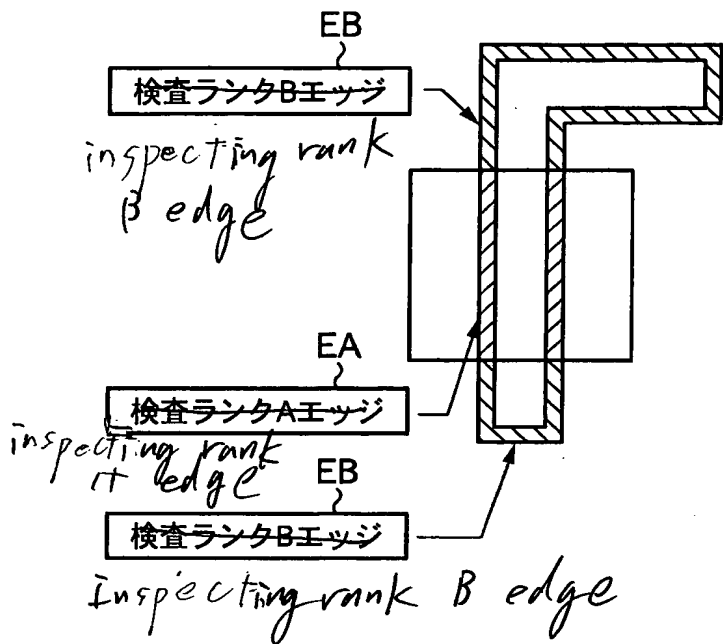


【図7】

Fig. 7

○エッジで指定する場合

In the case in which specification is carried out by edge



【図8】

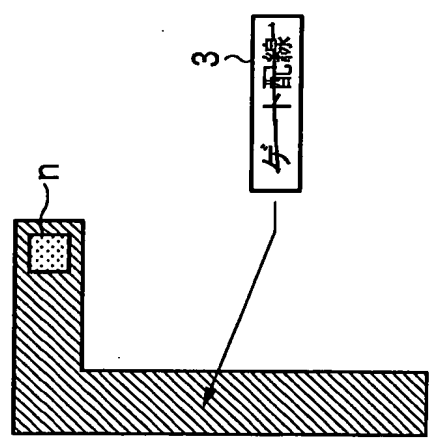


Fig. 8A

In the case in which specification is carried out by region
○領域で指定する場合

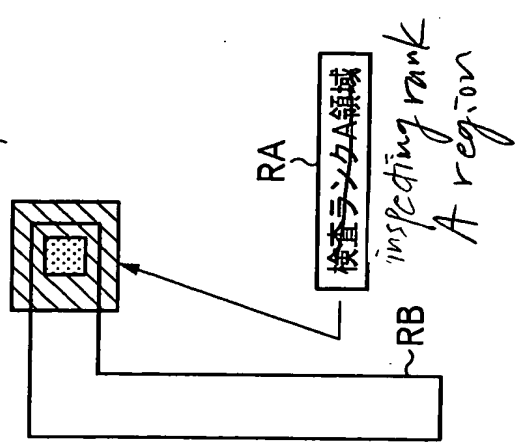


Fig. 8B

Fig. 8C

In the case in which specification is carried out by pattern
○パターンで指定する場合

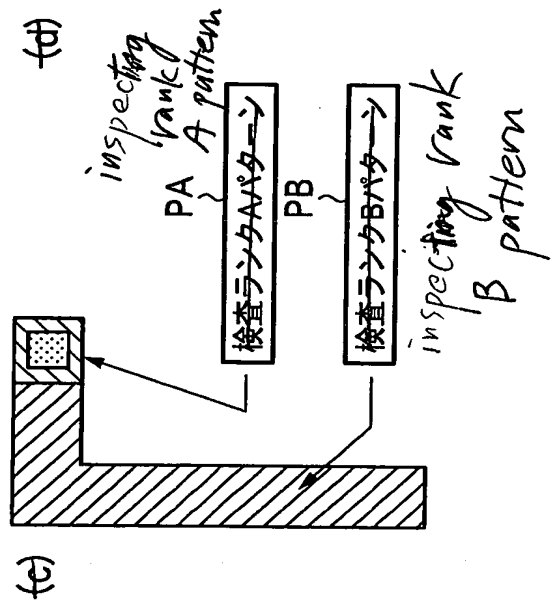
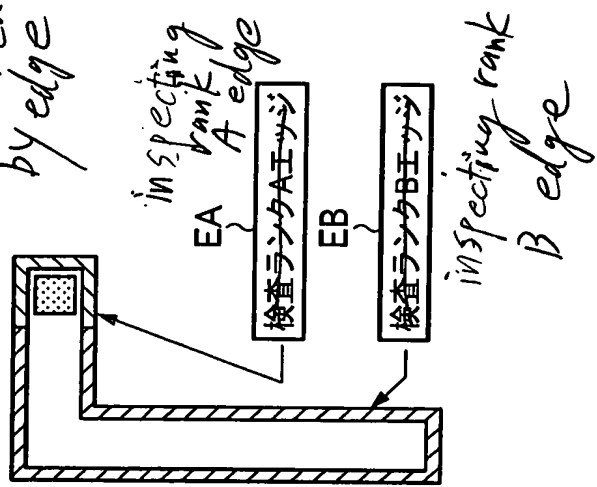


Fig. 8D In the case in which specification is carried out by edge
○エッジで指定する場合



【図9】

Fig-9A

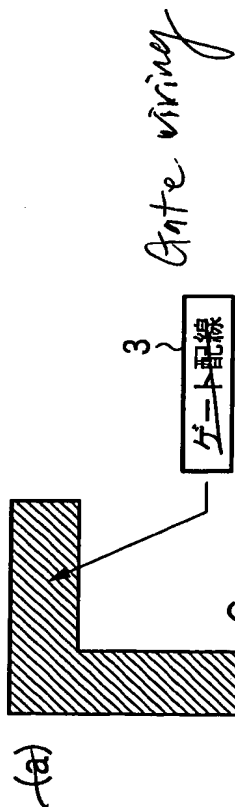


Fig. 9C

In the case in which specification is carried out by region
○領域で指定する場合

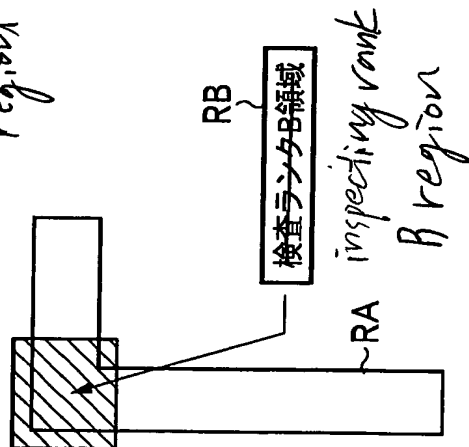


Fig. 9B

In the case in which specification is carried out by pattern
○パターンで指定する場合

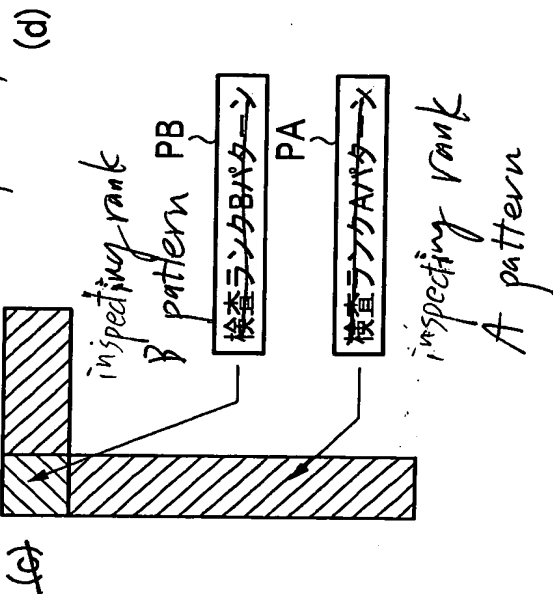
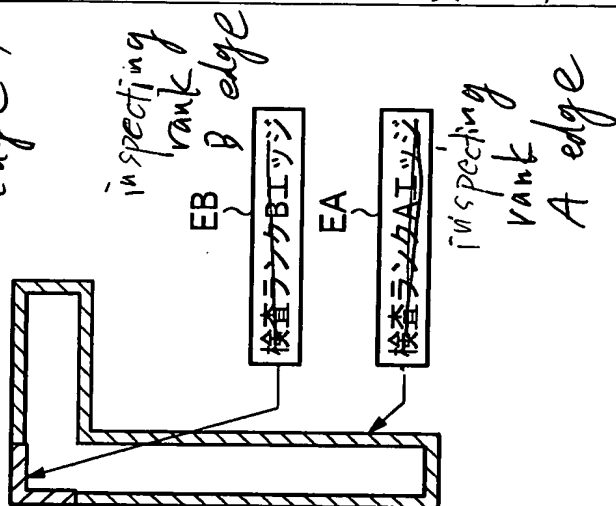


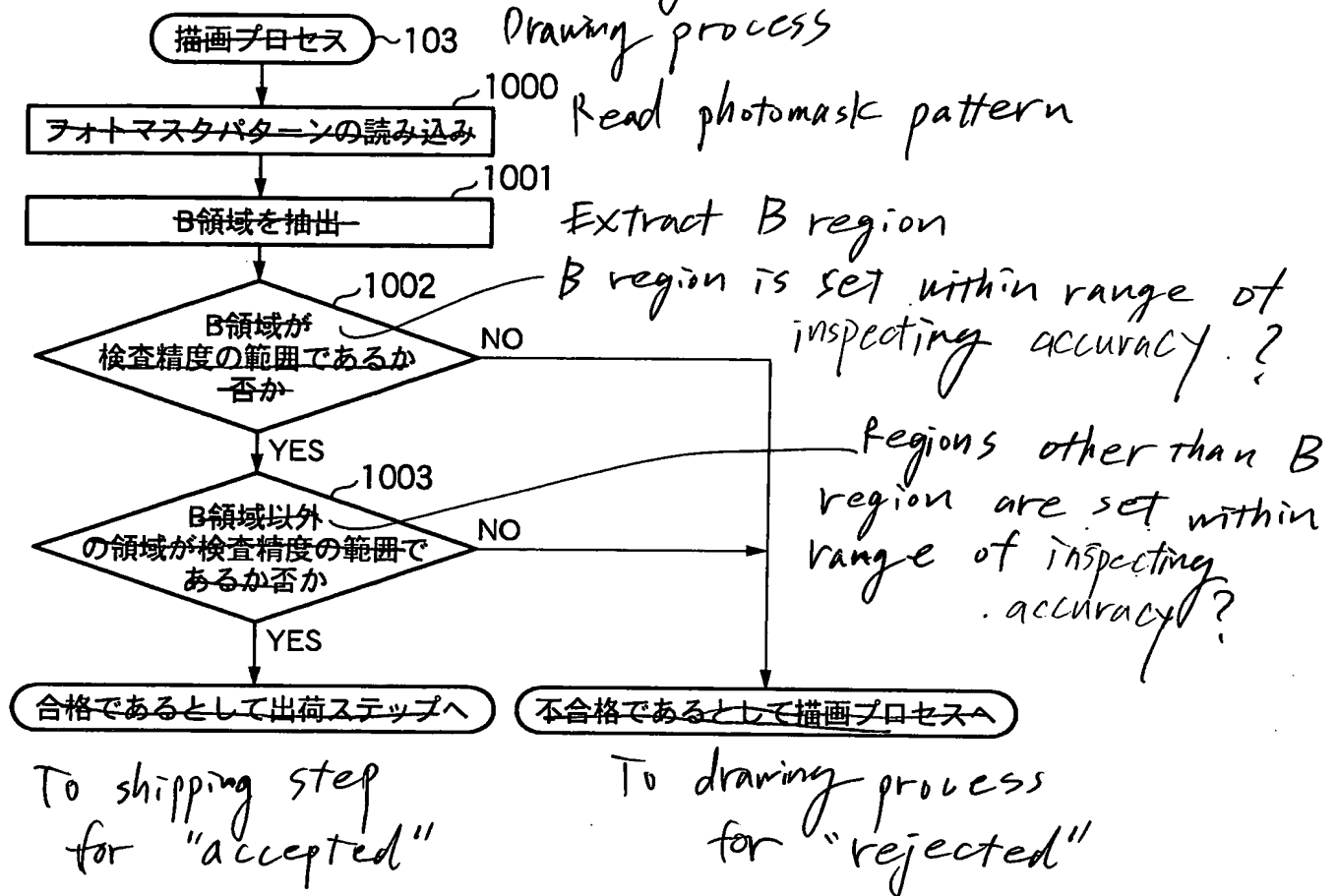
Fig. 9D

In the case in which specification is carried out by edge
○エッジで指定する場合



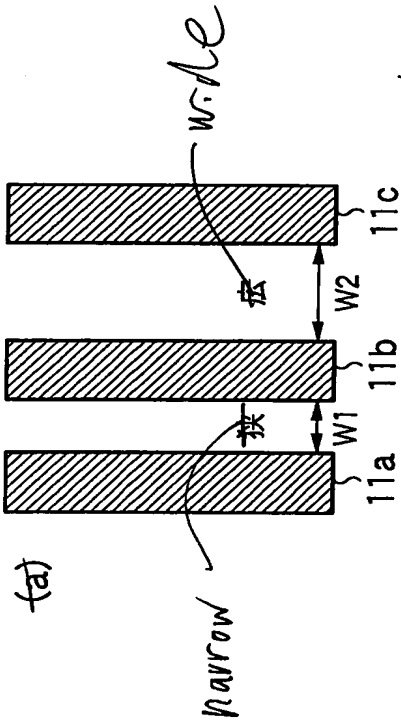
【図10】

Fig. 10



【図11】

Fig. 11A



In the case in which specification is carried out by region
○領域で指定する場合

Fig. 11B

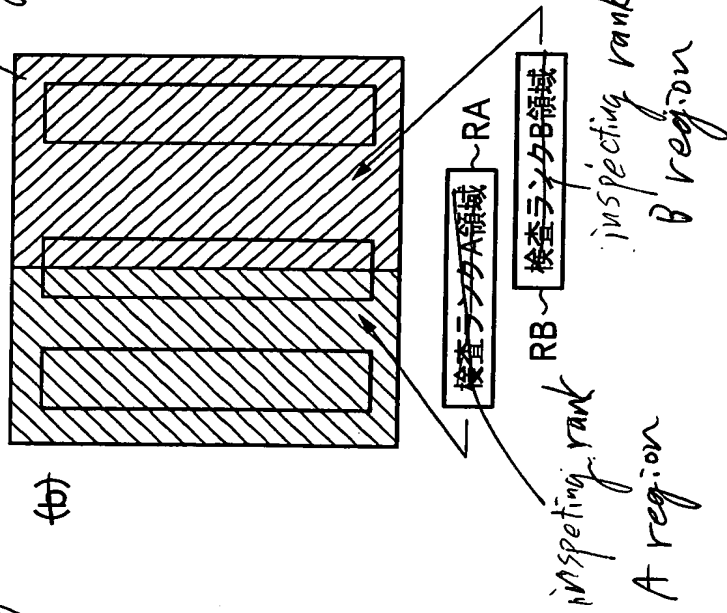


Fig. 11C

In the case in which specification is carried out by pattern
○パターンで指定する場合

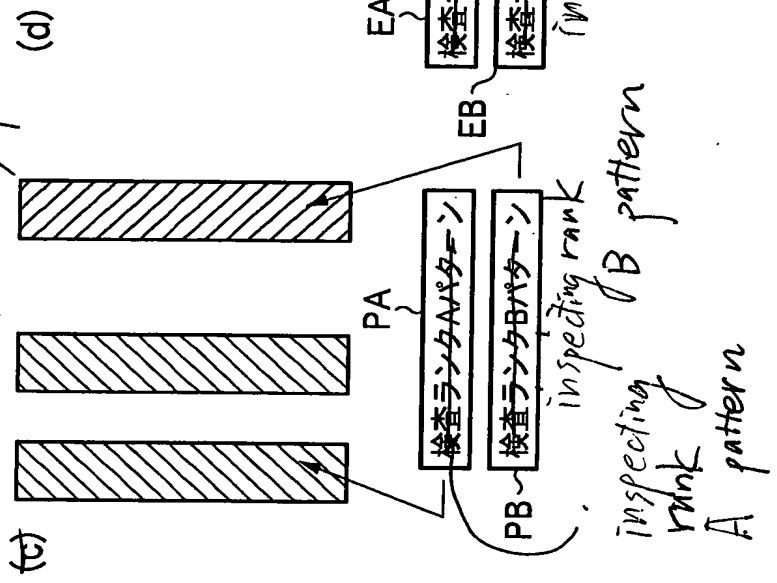
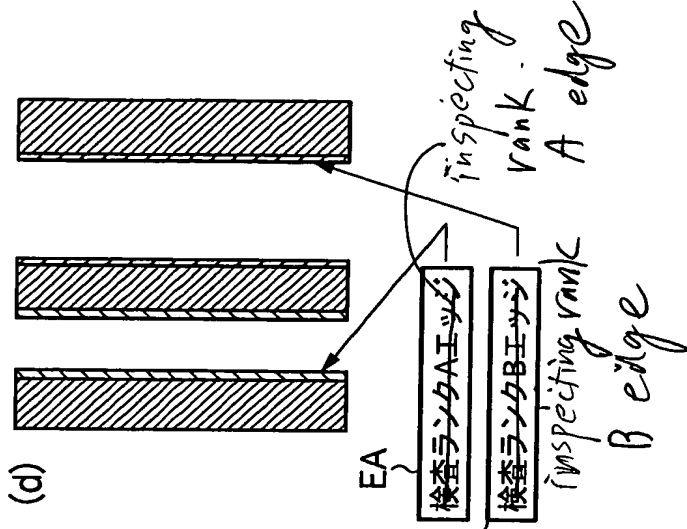


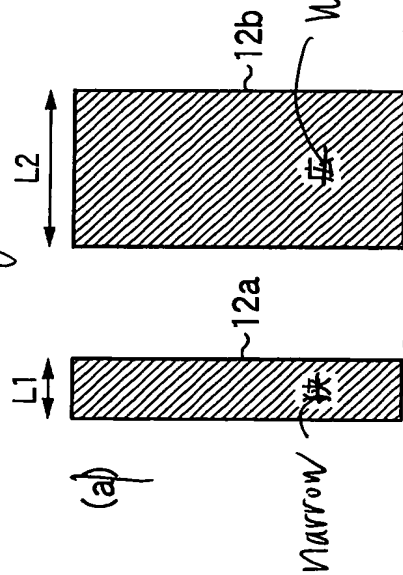
Fig. 11D

In the case in which specification is carried out by edge
○エッジで指定する場合



【図12】

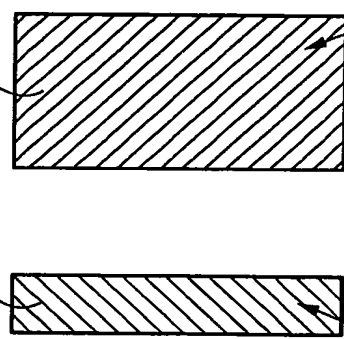
Fig. 12 A



In the case in which
○領域で指定する場合
is carried out by region

Fig. 12 C

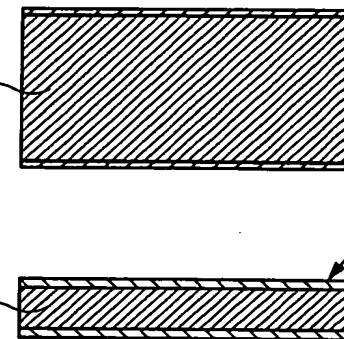
In the case in which
○エッジで指定する場合
is carried out by pattern



PA { 検査ランクAパターン }
PB { 検査ランクBパターン }
inspecting rank A pattern
inspecting rank B pattern

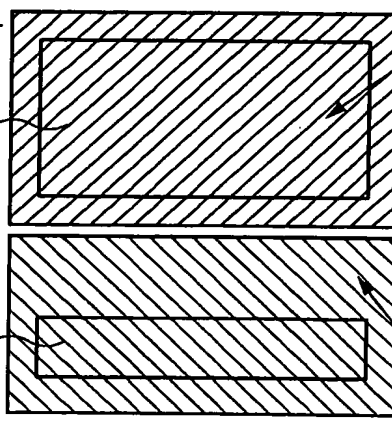
Fig. 12 D

In the case in which
○エッジで指定する場合
is carried out by pattern



EA { 検査ランクAエッジ }
EB { 検査ランクBエッジ }
inspecting rank A edge
inspecting rank B edge

Fig. 12 B



RB { 検査ランクA領域 }
RA { 検査ランクB領域 }
inspecting rank A region
inspecting rank B region

【図13】

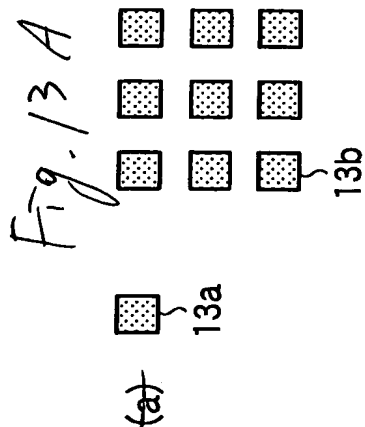


Fig. 13B In the case in which specification is carried out by region

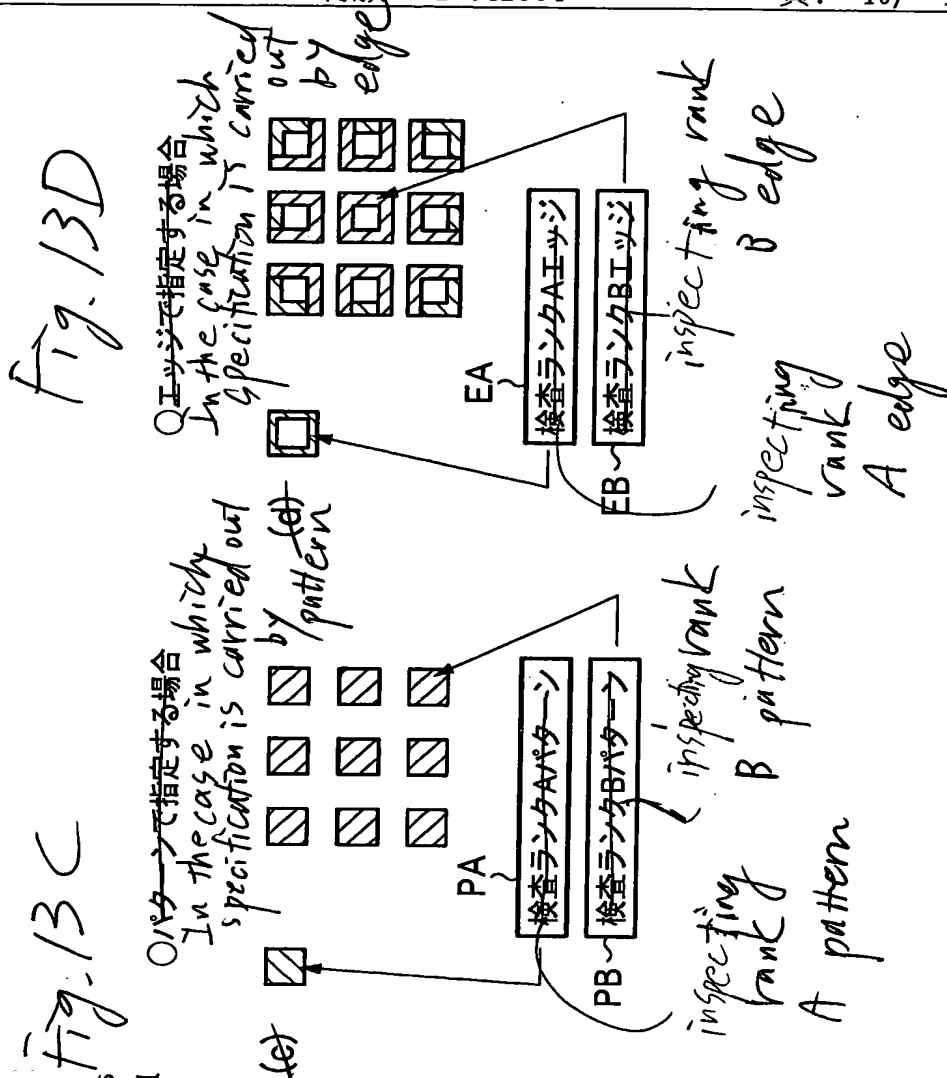
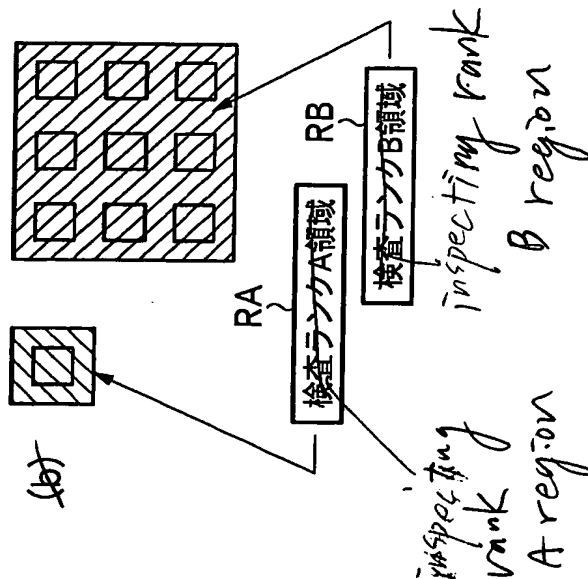
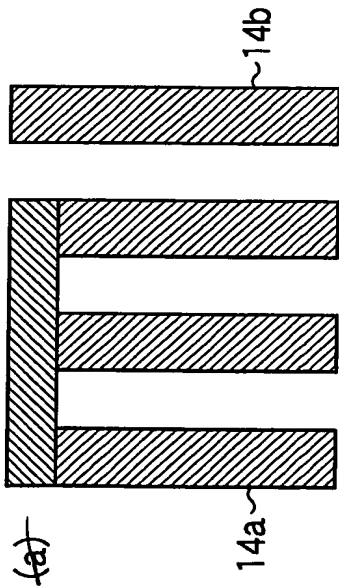
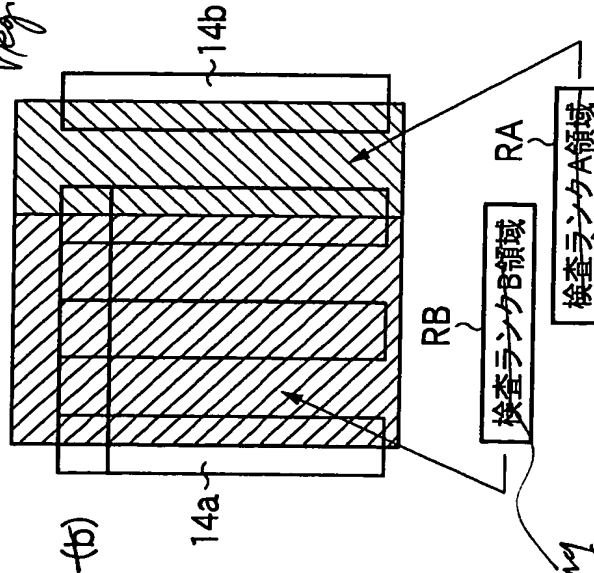


Fig. 14A



In the case in which specification is carried out by region

Fig. 14B

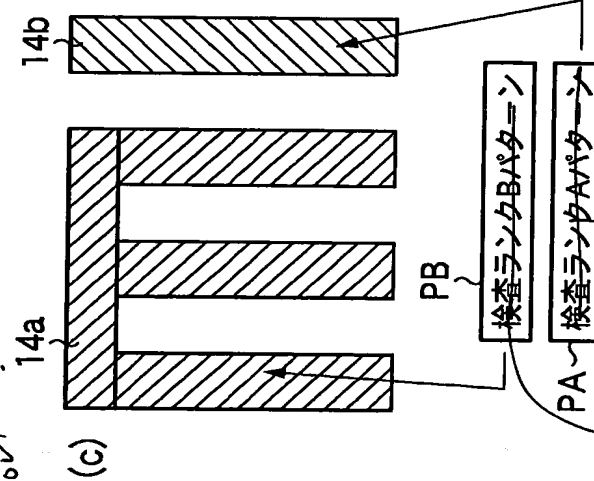


inspecting rank B region

inspecting rank A region

Fig. 14C

In the case in which specification is carried out by pattern

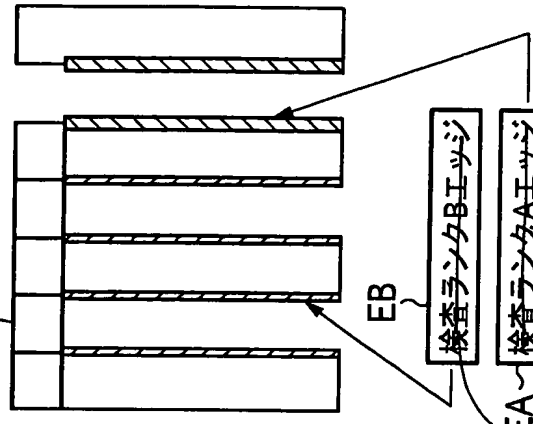


inspecting rank B pattern

inspecting rank A pattern

Fig. 14D

○エッジで指定する場合
In the case in which specification is carried out by edge

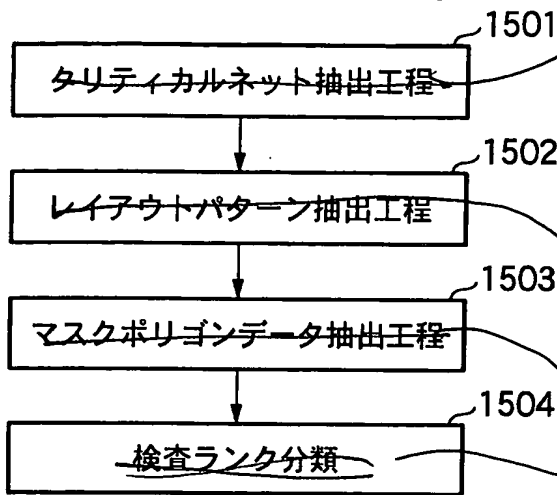


inspecting rank B edge

inspecting rank A edge

【図15】

Fig. 15



Critical net extracting step

タリティカルの例

- ・クロックネット
- ・タイミング制約設定ネット
- ・アナログネット
- (抵抗値・容量の精度が要求される)
- ・高速信号ネット etc

Example of critical

・ Clock net

・ Timing constraint

Setting net

・ Analog net (precision in resistance value and capacity is required)

・ High-speed signal net etc

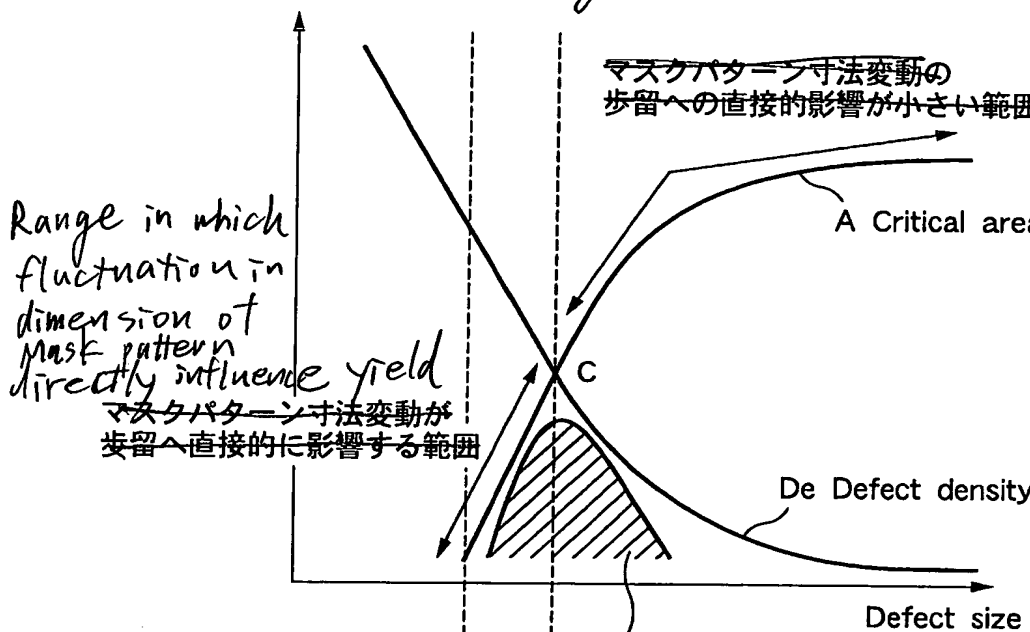
Layout pattern extracting step

Mask polygon data extracting step

inspecting rank classification

【図16】

Fig. 16



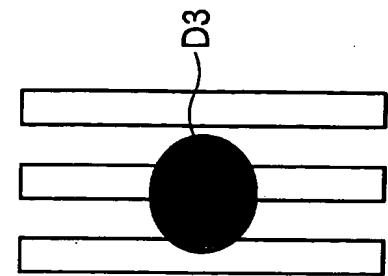
Range in which direct influence of fluctuation in dimension of mask pattern on yield is small

Minimum design rule (2002年量産ベースで130nm) (on mass production basis in 2002)

Threshold of inspecting accuracy

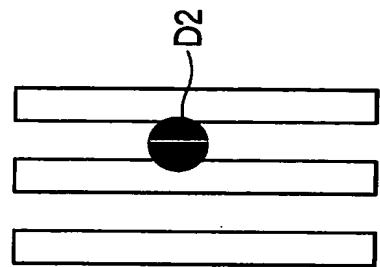
【図17】

Fig. 17C



(c)

Fig. 17B

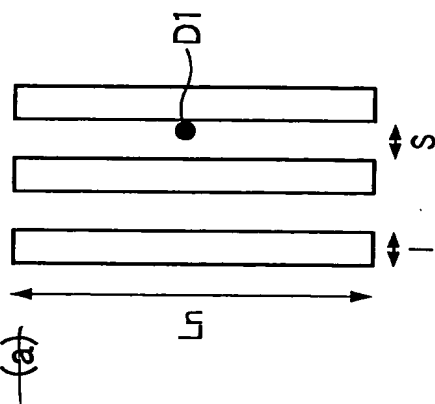


(b)

Fig. 17A

Defect

Short不良 Area = $L_n(I+S)$



(a)

Defect size $(x) < S$

No short defect ~~Short不良~~

$$Ca(x) = 0$$

$S < \text{Defect size } (x) < 2I+S$

場所によってはShort不良

Short defect in

$$Ca(x) = \frac{L_n(I+S)(X-S)}{(I+S)}$$

Some places

$2I+S < \text{Defect size } (x)$

必ずShort不良

$$Ca(x) = L_n(I+S)$$

Short defect in all places

【図18】

Fig. 18A

(a)

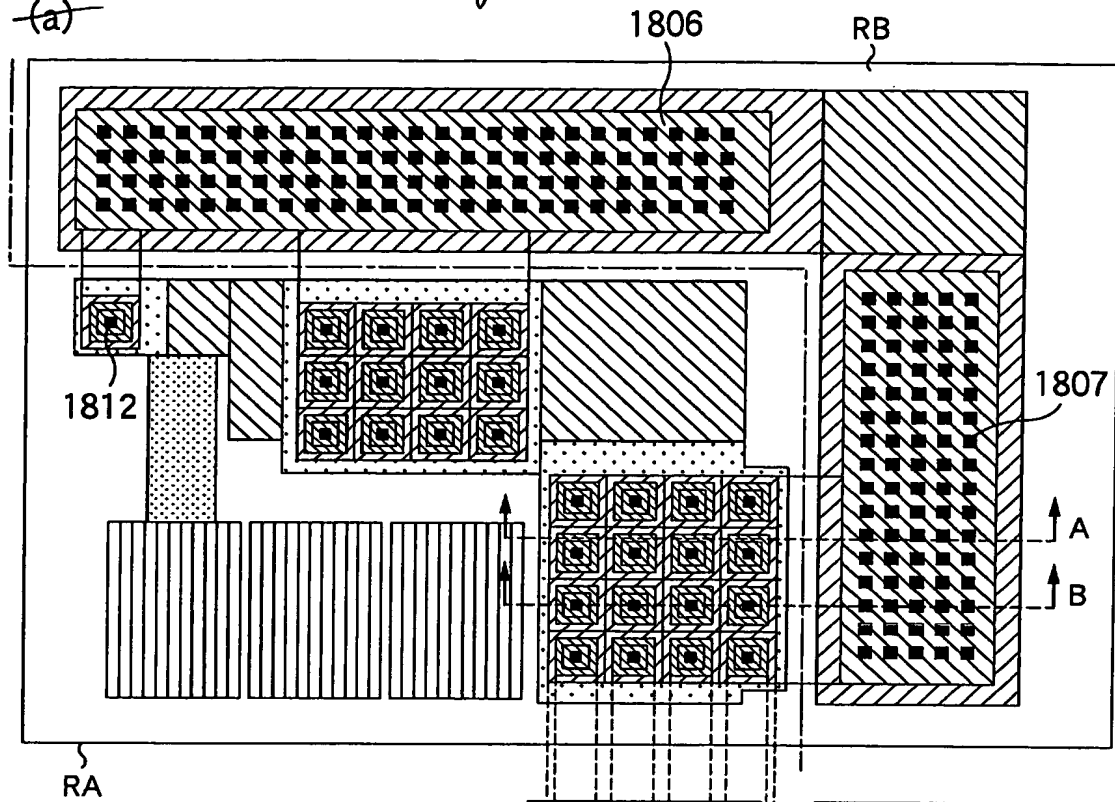


Fig. 18B(b) A断面
A section

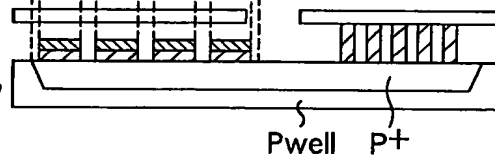
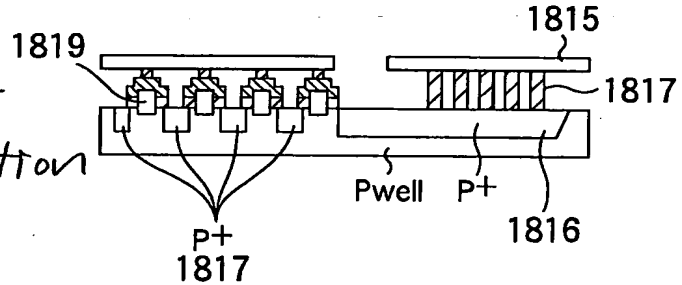


Fig. 18C(c) B断面
B section



【図19】

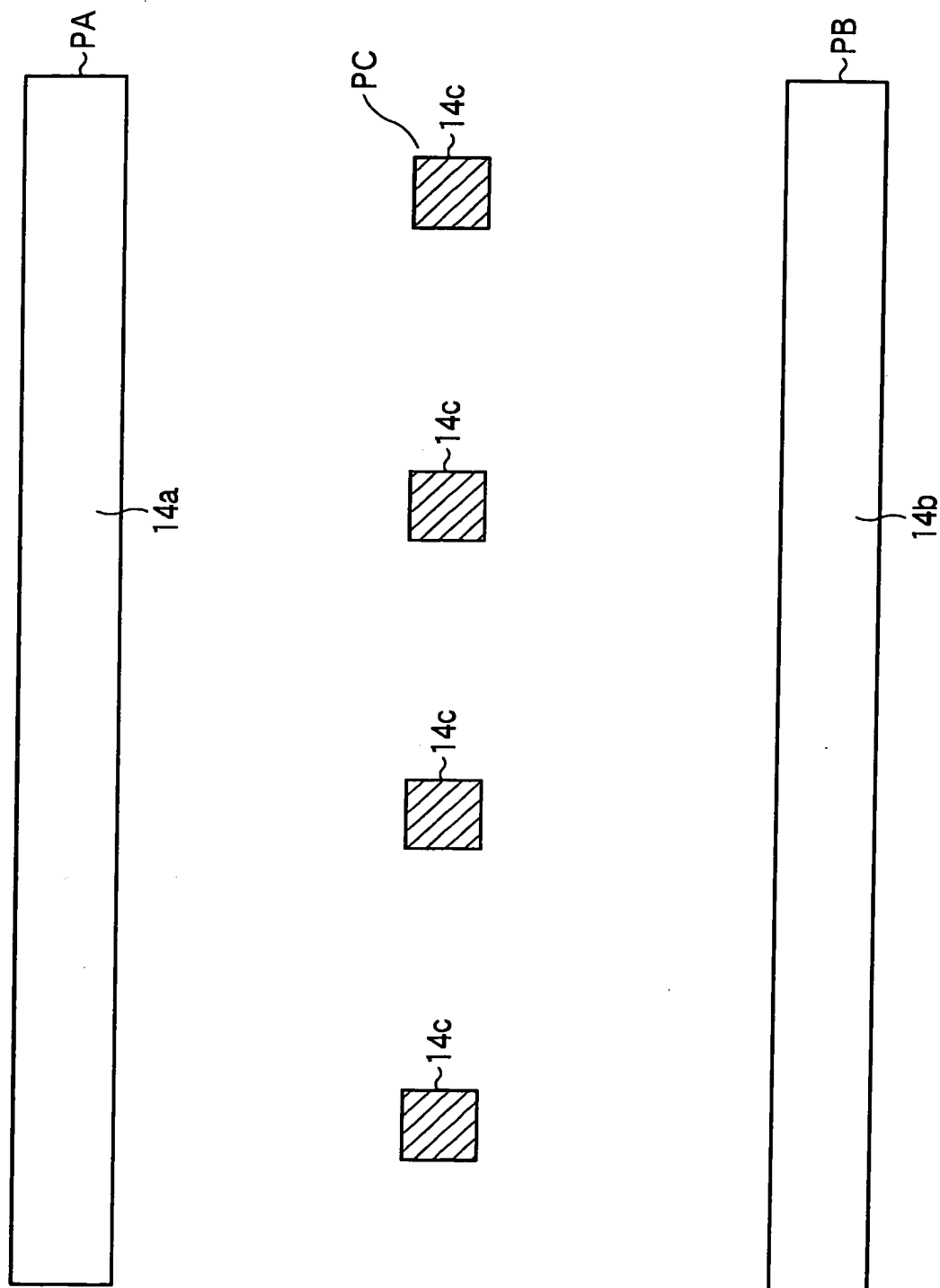
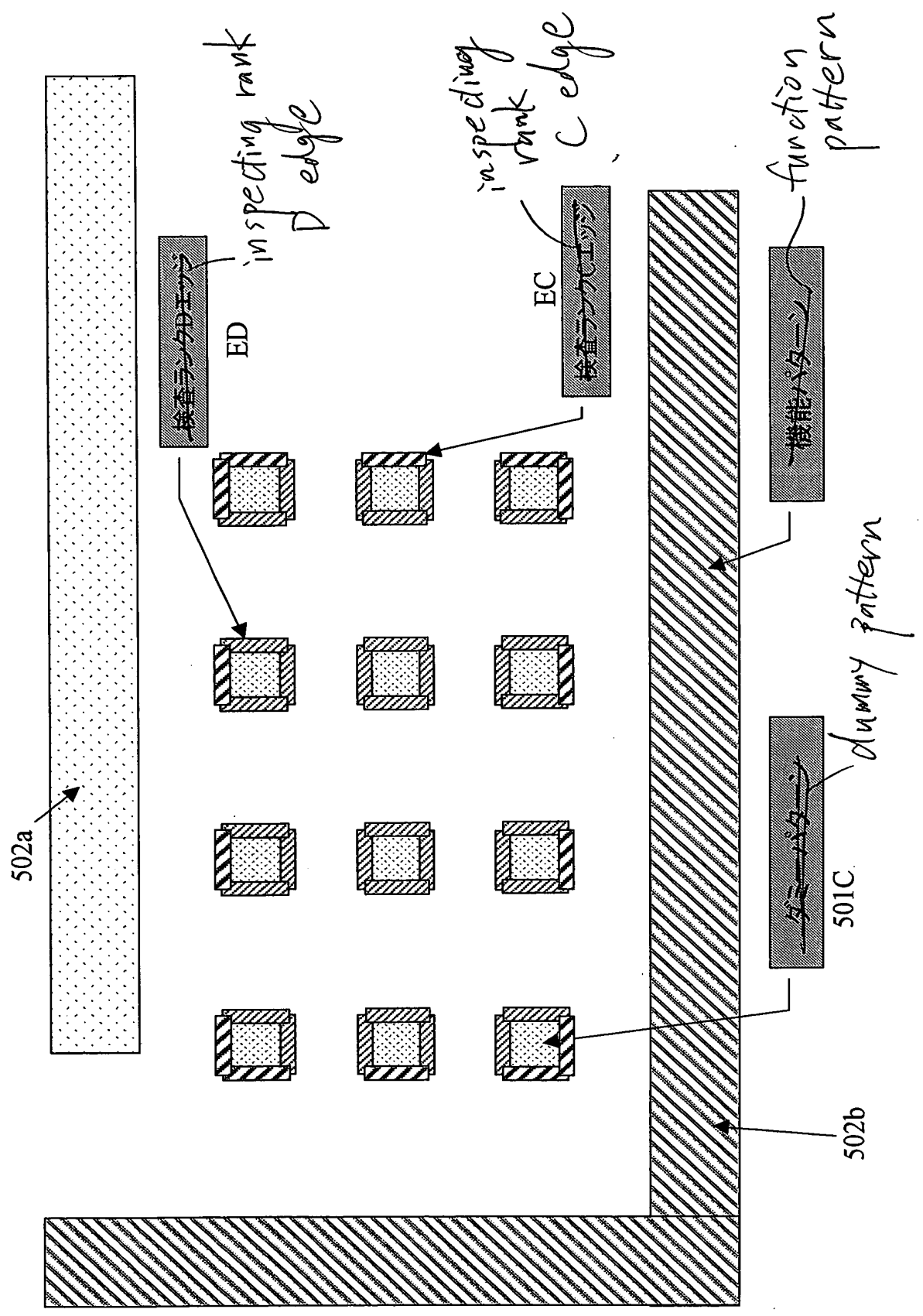


Fig. 19

ダミーパターンの位置関係による分類

Fig-20

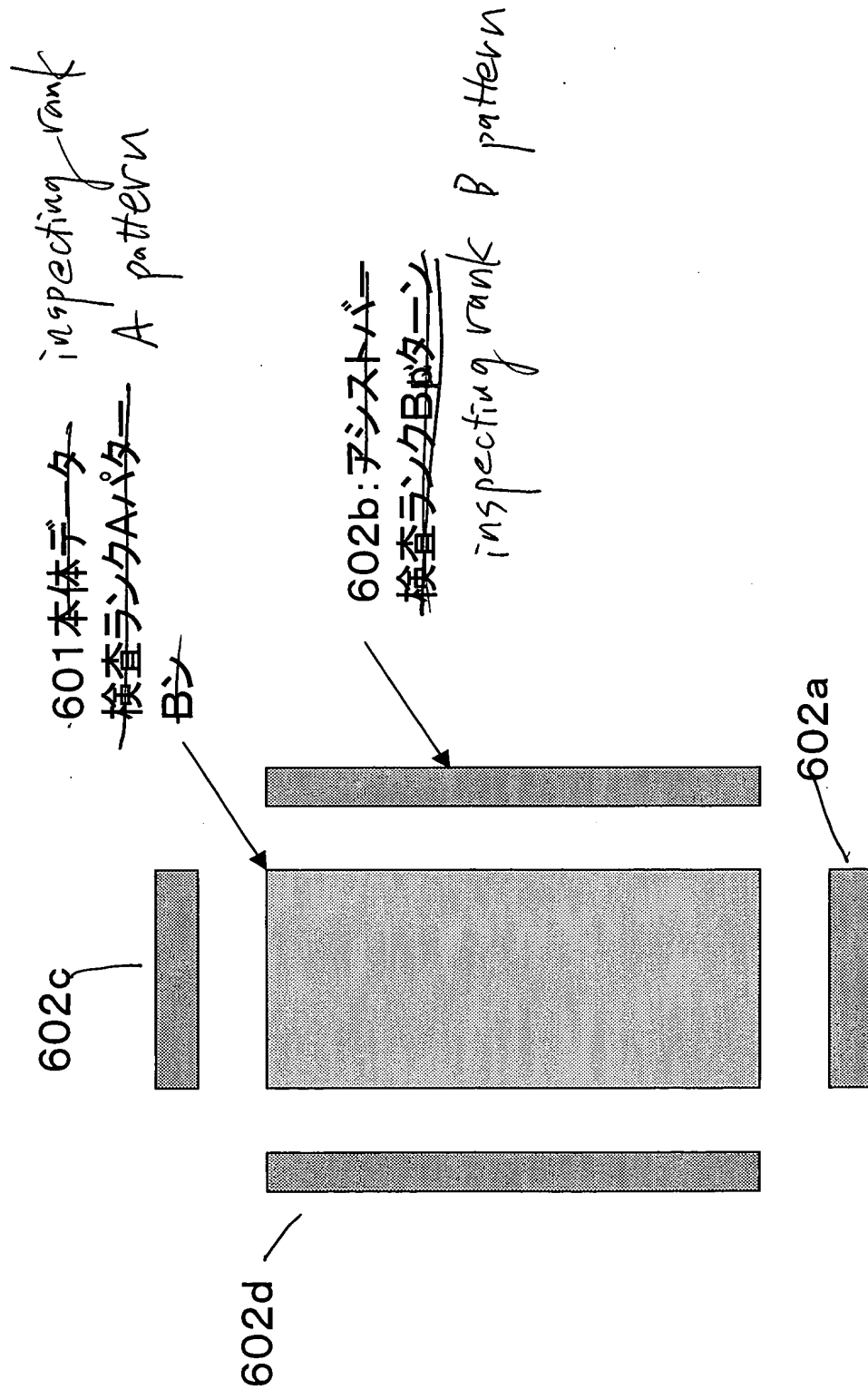
図20。



アシストバーへの適用例

図21

Fig. 21



位相シフトマスク(エンハンサー)への適用例

図22

Fig. 22

702C

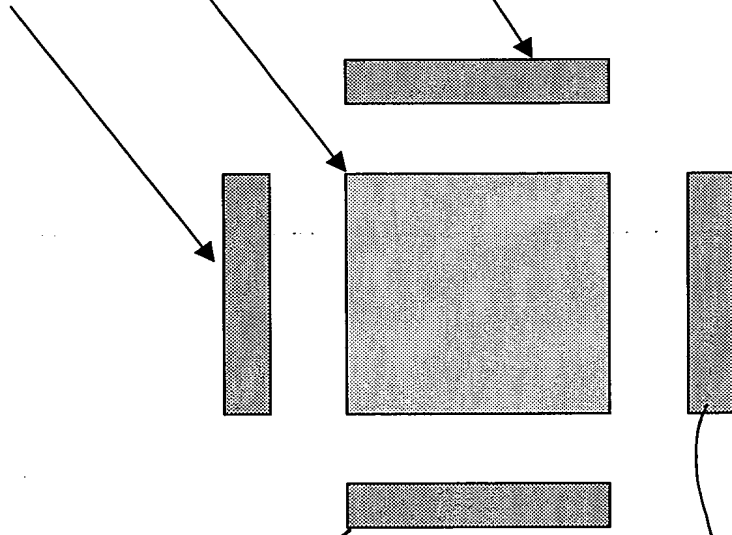
701:メイン開口部(本体パターン)
ガラスの掘り込みによって
180°位相がシフトした開口部
(開口部以外と360°ずれた同位相)

702b:サブ開口部
0°の開口部

開口部以外
180°のハーフトニシ膜

702d

702a



~~位相シフトマスク(エンハンサー)への適用例~~

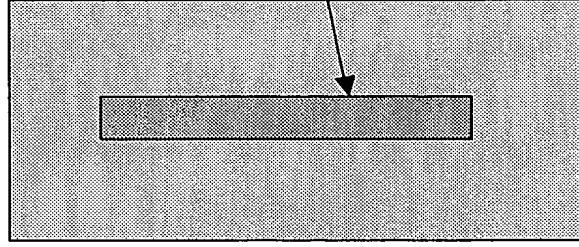
• ~~図23~~

Fig. 23

~~801:遮光部(本体パターン)~~

~~802:180°の位相シフター~~

~~本体パターン以外
0°の開孔~~



位相シフトマスク(CPL)への適用例

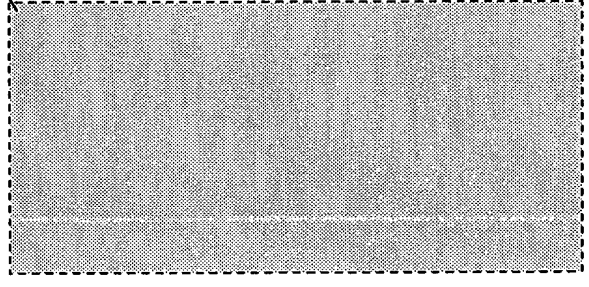
図24

Fig. 24A

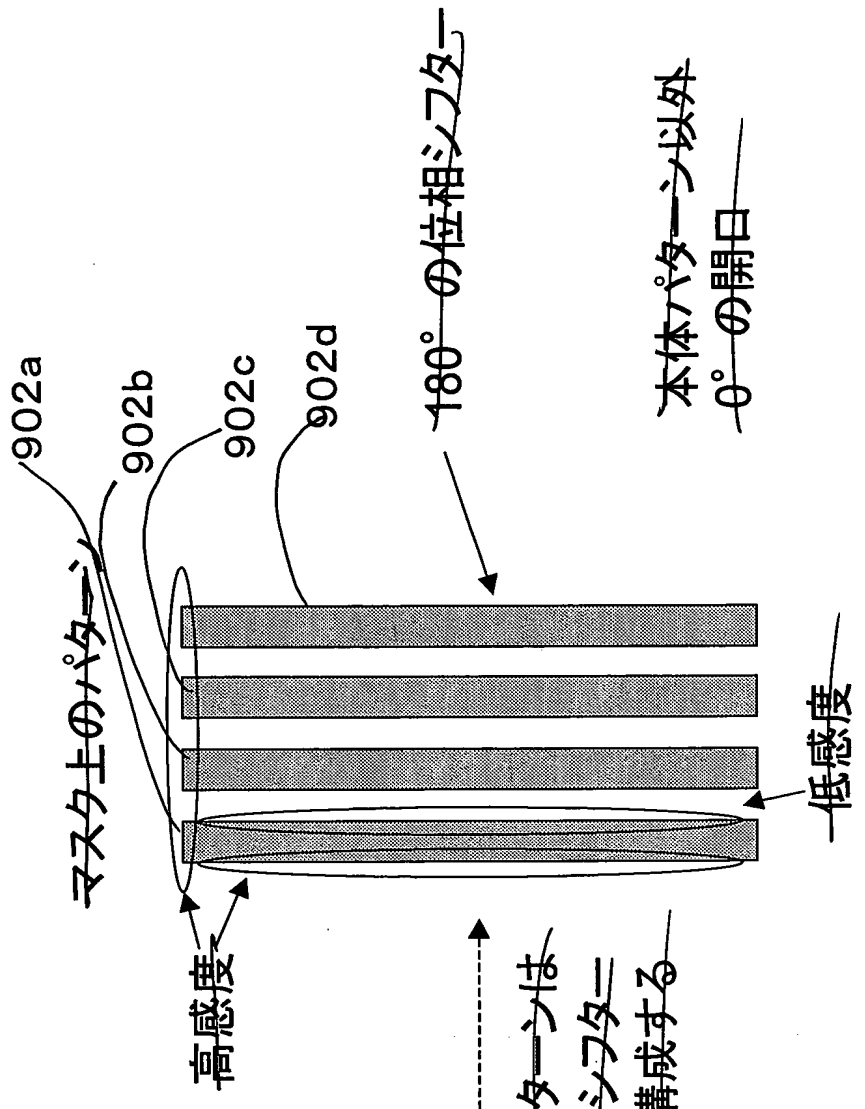
Fig. 24B

解像したい本体パターン

901

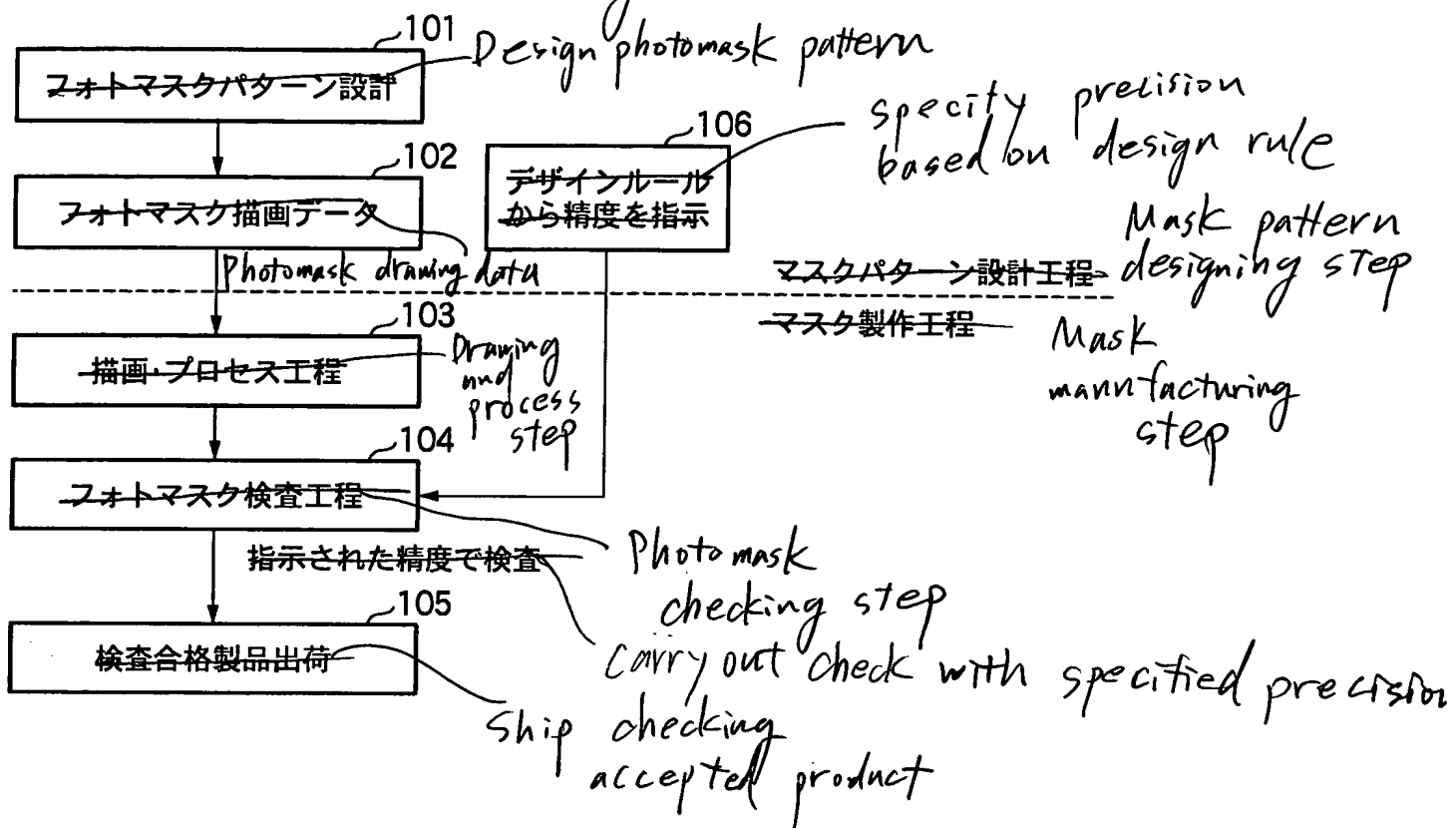


太いパターンは
複数のシフト
により構成する



【図20】

Fig. 25

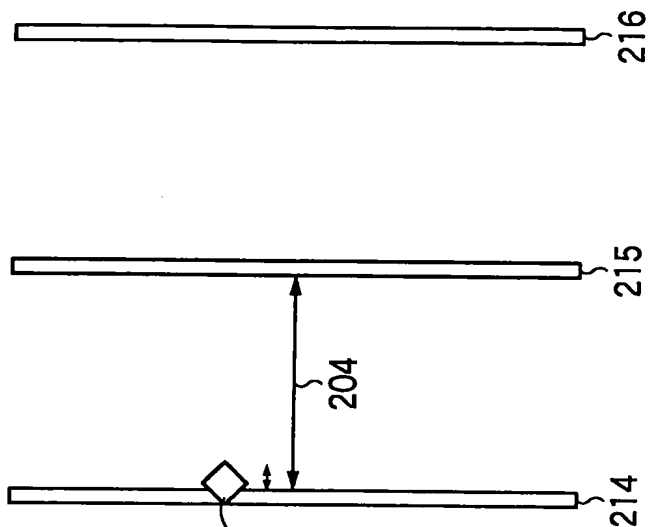


【図21】

(b) 配線間隔の広い配線時の欠陥

Fig. 26B

Defect in wiring with large wiring interval



(a) 最小間隔の配線時の欠陥

Fig. 26A

Defect in wiring with minimum interval

